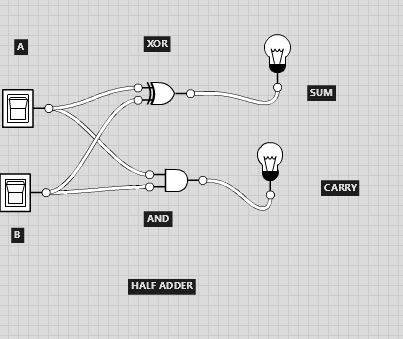
**LAB 6-8**

**1. Design Half Adder and Full Adder along with truth tables.**

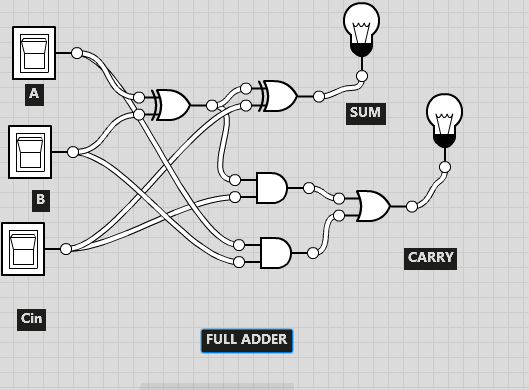
**HALF ADDER:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **∑** | **C** |
| **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** |

****

**FULL ADDER:**

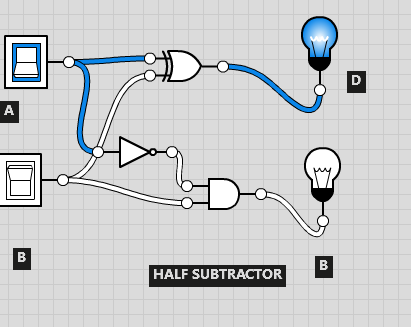
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Cin | Cout | Sum |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |



**2. Design Half Subtractor and Full Subtractor along with truth tables.**

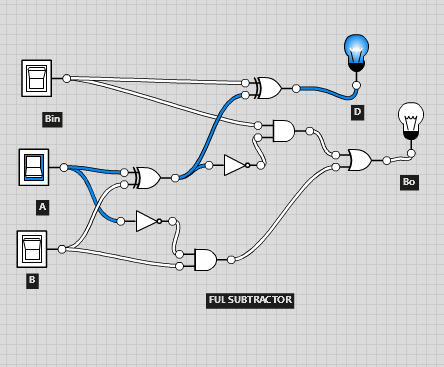
**HALF SUBTRACTOR:**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **D** | **B** |
| **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **0** |
|  |  |  |  |



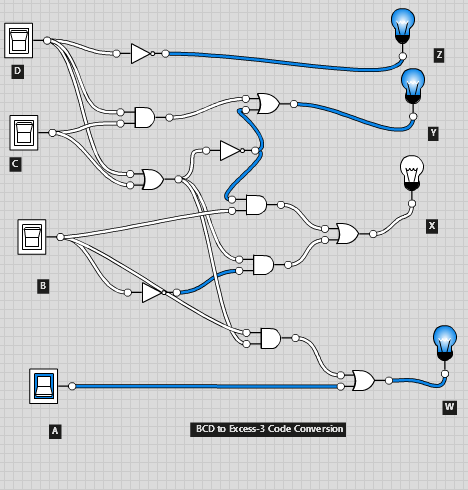
**FULL SUBTRACTOR:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **Bin** | **D** | **Bout** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **1** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** |



**3. Design BCD to Excess-3 Code Converter with truth table.**

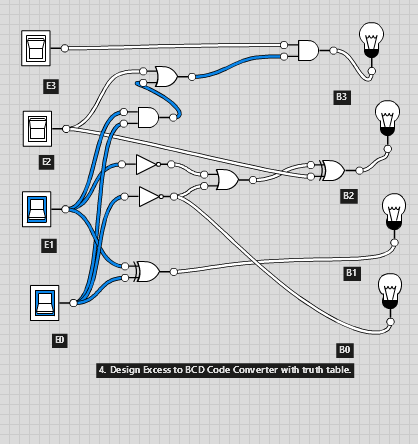
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **W** | **X** | **Y** | **Z** |
| **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **1** | **1** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** | **1** | **1** | **1** |
| **0** | **1** | **0** | **1** | **1** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **1** | **1** | **1** | **0** | **1** | **0** |
| **1** | **0** | **0** | **0** | **1** | **0** | **1** | **1** |
| **1** | **0** | **0** | **1** | **1** | **1** | **0** | **0** |
| **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **1** | **1** | **1** | **1** | **1** | **0** |
| **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** |
| **1** | **1** | **0** | **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **1** | **0** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** |



4. **Design Excess to BCD Code Converter with truth table.**

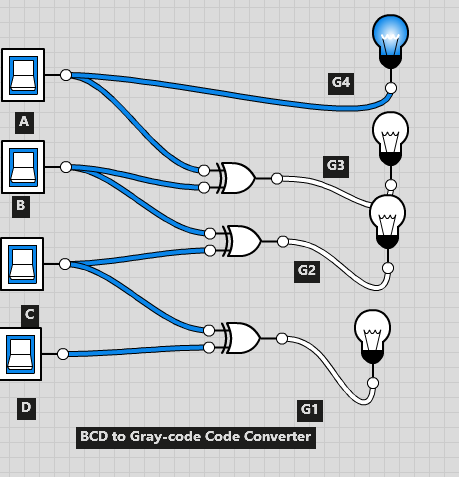
|  |  |
| --- | --- |
| **Excess-3** | **BCD OUTPUT** |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **E3** | **E2** | **E1** | **E0** | **B3** | **B2** | **B1** | **B0** |
| **0** | **0** | **0** | **0** | **X** | **X** | **X** | **X** |
| **0** | **0** | **0** | **1** | **X** | **X** | **X** | **X** |
| **0** | **0** | **1** | **0** | **X** | **X** | **X** | **X** |
| **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **0** | **0** | **1** | **1** |
| **0** | **1** | **1** | **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **0** | **0** | **0** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** | **1** | **1** | **0** |
| **1** | **0** | **1** | **0** | **0** | **1** | **1** | **1** |
| **1** | **0** | **1** | **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **0** | **1** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **X** | **X** | **X** | **X** |
| **1** | **1** | **1** | **0** | **X** | **X** | **X** | **X** |
| **1** | **1** | **1** | **1** | **X** | **X** | **X** | **X** |



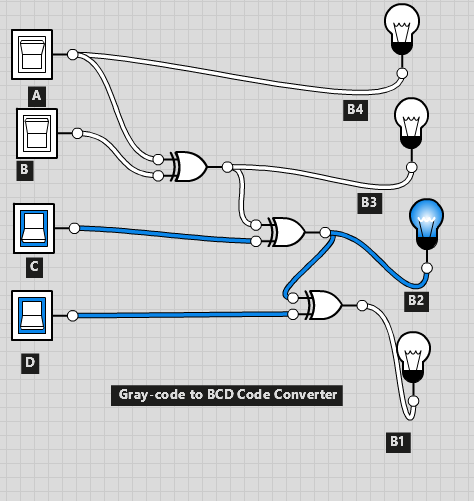
5. **Design BCD to Gray-code Code Converter with truth table**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **G1** | **G2** | **G3** | **G4** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **1** | **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** | **1** | **1** | **1** |
| **0** | **1** | **1** | **0** | **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **0** | **0** | **1** | **1** | **0** | **0** |
| **1** | **0** | **0** | **1** | **1** | **1** | **0** | **1** |
| **1** | **0** | **1** | **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **1** | **1** | **1** | **1** | **1** | **0** |
| **1** | **1** | **0** | **0** | **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** |



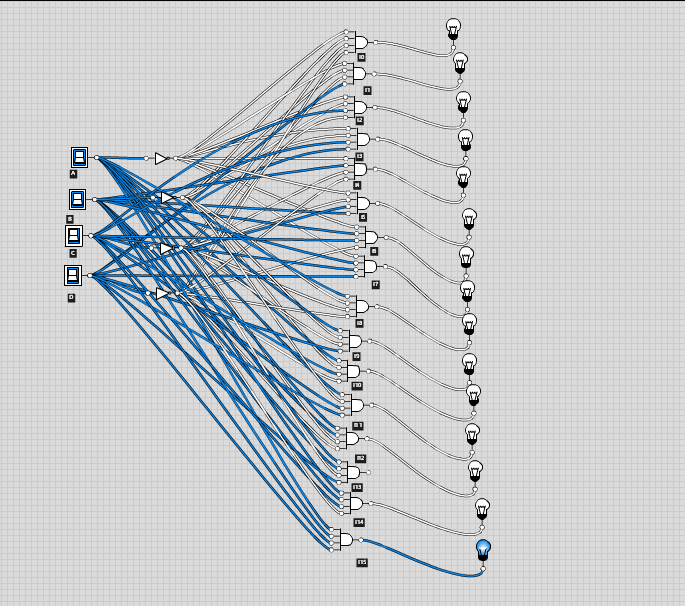
6. **Design Gray-code to BCD Code Converter truth table.**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **B4** | **B3** | **B2** | **B1** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **0** | **0** | **0** | **1** |
| **0** | **0** | **1** | **1** | **0** | **0** | **1** | **0** |
| **0** | **0** | **1** | **0** | **0** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **0** | **1** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** | **1** | **1** | **1** |
| **1** | **1** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **1** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **1** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** | **1** | **1** | **1** | **1** |



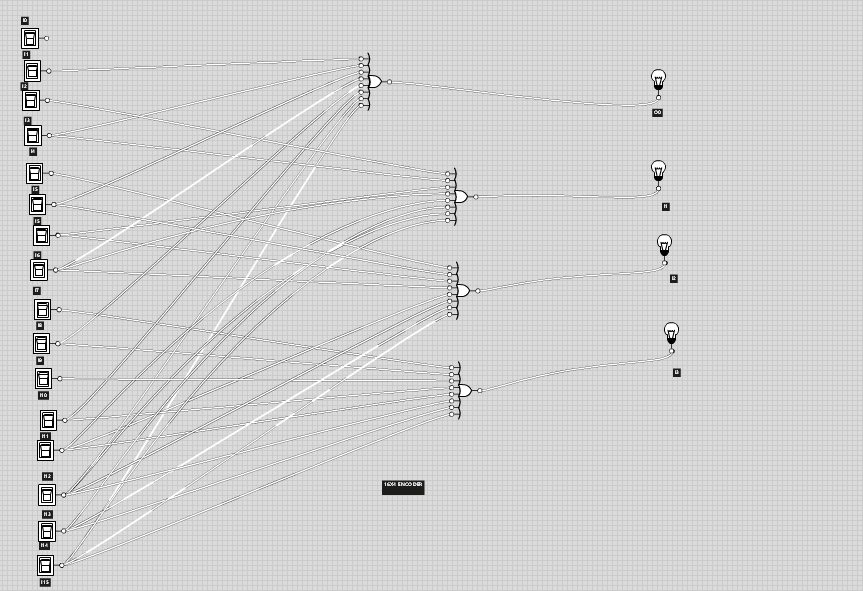
**7. Design 16:1 mux using basic gates**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **INPUT** |
| **0** | **0** | **0** | **0** | **I0** |
| **0** | **0** | **0** | **1** | **I1** |
| **0** | **0** | **1** | **0** | **I2** |
| **0** | **0** | **1** | **1** | **I3** |
| **0** | **1** | **0** | **0** | **I4** |
| **0** | **1** | **0** | **1** | **I5** |
| **0** | **1** | **1** | **0** | **I6** |
| **0** | **1** | **1** | **1** | **I7** |
| **1** | **0** | **0** | **0** | **I8** |
| **1** | **0** | **0** | **1** | **I9** |
| **1** | **0** | **1** | **0** | **I10** |
| **1** | **0** | **1** | **1** | **I11** |
| **1** | **1** | **0** | **0** | **I12** |
| **1** | **1** | **0** | **1** | **I13** |
| **1** | **1** | **1** | **0** | **I14** |
| **1** | **1** | **1** | **1** | **I15** |



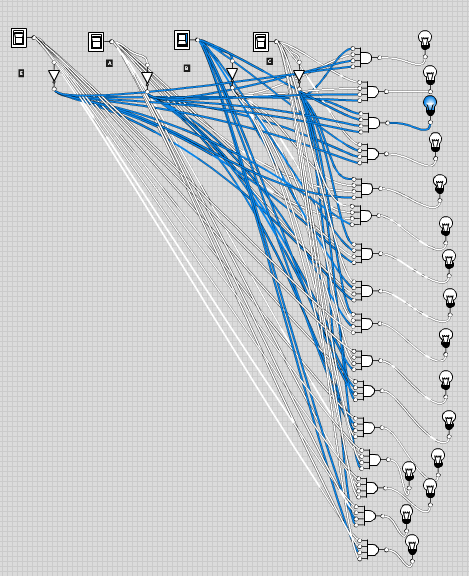
**8. Design 16:4 encoder using basic gates**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **I15** | **I14** | **I13** | **I12** | **I11** | **I10** | **I9** | **I8** | **I7** | **I6** | **I5** | **I4** | **I3** | I2 | **I1** | **I0** | **03** | **02** | **01** | **00** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **1** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** |
| **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** |
| **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **1** |
| **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0** |
| **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** |



**9. Design 4:16 decoder using basic gates**

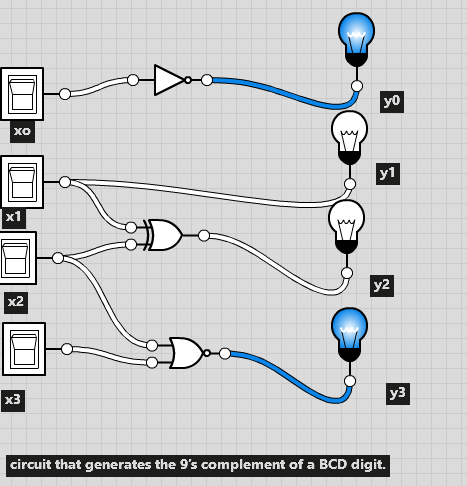
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| E | A | B | C | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 | Y8 | Y9 | Y10 | Y11 | Y12 | Y13 | Y14 | Y15 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |



**Lab: 9-10**

**1. Design a combinational circuit that generates the 9’s complement of a BCD digit.**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **X3** | **X2** | **X1** | **X0** | **Y3** | **Y2** | **Y1** | **Y0** |
| **0** | **0** | **0** | **0** | **1** | **0** | **0** | **1** |
| **0** | **0** | **0** | **1** | **1** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** | **0** | **1** | **1** | **1** |
| **0** | **0** | **1** | **1** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** |
| **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **0** | **0** | **0** | **1** | **1** |
| **0** | **1** | **1** | **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |



**2. A combinational circuit is defined by the following functions, Design the circuit with the decoder and external gates.**

**F1 = A’B’+AB’C+A’BC+C+AB’+C’+AB**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **F** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**XOR**

A

DO

D1

D2

D3

B

C

**F2 = AB’C’D+AC’D+C’D+C’D+A’B+AD**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **0** | **1** | **1** | **1** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** |

D

C

B

**A**

D0

D1

D2

D3

D4

D5

D6

D7

D8

D9

D10

D11

D12

D13

D14

D15

**XOR**

**F3=AB+A’C’D+A’BD+AB’C’**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **0** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** |

A

XOR

D0

D1

D2

D3

D4

D5

D6

D7

D8

D9

D10

D11

D12

D13

D14

D15

D

C

B

**3. A combinational circuit is defined by the following functions, Design the circuit with the multiplexers and external gates.**

**F1 = A’B’+AB’C+A’BC+C+AB’+C’+AB**

|  |  |  |  |
| --- | --- | --- | --- |
| **A** | **B** | **C** | **F** |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **I0** | **I1** | **I2** | **I3** |
| **C’** | 0 | 2 | 4 | 6 |
| **C** | 1 | 3 | 5 | 7 |

**1 1 1 1**

**1**

**I0**

**I1 Y**

**I2**

**I3**

Y

A

B

**F2 = AB’C’D+AC’D+C’D+C’D+A’B+AD**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **1** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **0** | **1** | **1** | **1** |
| **1** | **1** | **0** | **0** | **0** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** | **1** |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **I0** | **I1** | **I2** | **I3** | **I4** | **I5** | **I6** | **I7** |
| **D’** | **0** | **2** | **4** | **6** | **8** | **10** | **12** | **14** |
| **D** | **1** | **3** | **5** | **7** | **9** | **11** | **13** | **15** |

**D 0 1 1 D 1 D D**

I0

I2

I3

I4

I5

I6

I7 Y

D

0

1

A B C

**F3=AB+A’C’D+A’BD+AB’C’**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **F** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **0** | **1** | **1** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **0** | **0** |
| **0** | **1** | **0** | **1** | **1** |
| **0** | **1** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** | **1** |
| **1** | **0** | **0** | **1** | **1** |
| **1** | **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **1** | **0** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **I0** | **I1** | **I2** | **I3** | **I4** | **I5** | **I6** | **I7** |
| **D’** | **0** | **2** | **4** | **6** | **8** | **10** | **12** | **14** |
| **D** | **1** | **3** | **5** | **7** | **9** | **11** | **13** | **15** |

**D 0 D D 1 0 1 1**

I0

I1

I2

I3 Y

I4

I5

I6

I7

D

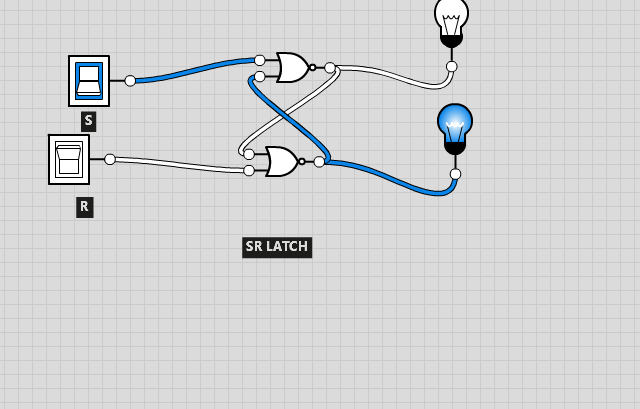
A B C

1

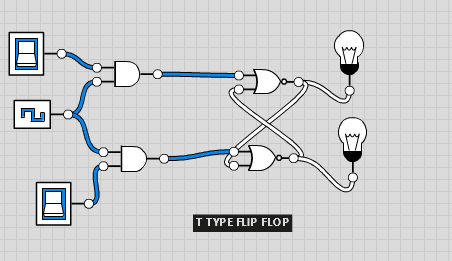
0

**LAB 9-13:**

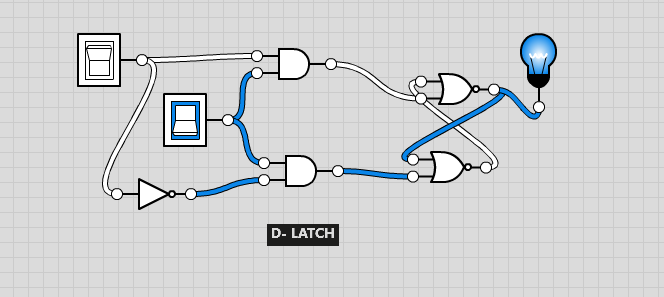
**RS flip flop**



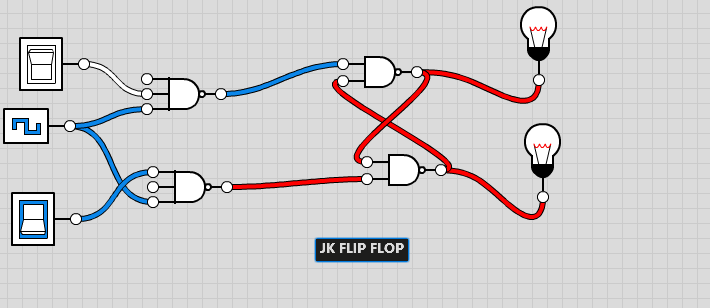
**T type flip flop**



**D type latch**



**JK flip flop**



**JK master flip flop**

